WHAT IS CLAIMED IS:

1. A display panel driving apparatus, comprising:

a display control section for controlling display on a display panel;

a drive section for driving the display panel on the basis of a signal supplied from the display control section; and

a data transfer device for transferring data between the display control section and the drive section,

wherein the drive section comprises a control signal conversion section for decoding signals supplied from the display control section, and generating drive pulse generation control signals.

2. The display panel driving apparatus according to claim 1, wherein the drive section further comprises a drive pulse generation circuit, wherein the drive pulse generation circuit comprises a plurality of switches that turn on/off according to a drive pulse generation control signal, and generates drive pulses for driving the display panel by using on/off of these switches.

3. A display panel driving apparatus comprising:

a display control section comprising a storage section for storing address data, a read section for reading address data stored in the storage section, and a shift clock generation section for generating a shift clock;

a drive section comprising a shift register for sequentially storing the address data according to the shift

clock, a latch enable generation section for generating a latch enable, and a driving circuit for driving a display panel with the address data stored in the shift register on the basis of the latch enable; and

a data transfer device for transferring data between the display control section and the drive section,

wherein the shift clock generation section generates the shift clock only during a period in which address data is being read from the storage section, and

the latch enable generation section generates the latch enable on the basis of the shift clock.

4. The display panel driving apparatus according to Claim 3, wherein the data transfer device comprises:

in the display control section, a parallel-to-serial converter for conducting parallel-to-serial conversion on the address data and the shift clock, and a transmission section for converting a serial signal resulting from parallel-to-serial conversion conducted in the parallel-to-serial converter to a signal conforming to a differential serial transmission system, and transferring a resultant signal toward the drive section via a transmission line; and

in the drive section, a reception section for receiving the address data and the shift clock transferred via the transmission line, and a serial-to-parallel converter for conducting serial-to-parallel conversion on the address data and the shift clock received by the reception section.